COMPLETE LISTING OF CLAIMS
IN ASCENDING ORDER WITH STATUS INDICATOR

(Claims 1-47 Canceled)

48. (Previously presented) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

H1

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode;

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device.

49. (Original) The method of claim 48 wherein said step of providing doped silicon regions further comprises forming a seven-region planar thyristor.

50. (Original) The method of claim 49 wherein said step of providing doped silicon regions further comprises forming a p-n-p-n-p-n-p planar thyristor.

51. (Original) The method of claim 50 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.

52. (Original) The method of claim 49 wherein said step of providing doped silicon regions further comprises forming two memory cells.

53. (Original) The method of claim 52 further comprising connecting a central

region of said seven-region planar thyristor to a shared row address line.

54. (Original) The method of claim 48 wherein said step of providing doped silicon regions further comprises forming one memory cell.

55. (Previously presented) A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

H1

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device.

56. (Previously presented) The method of claim 55 wherein said step of providing doped silicon regions further comprises forming a seven-region planar thyristor.

57. (Previously presented) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming a p-n-p-n-p-n-p planar thyristor.

58. (Previously presented) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.

59. (Previously presented) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming two memory cells.

60. (Previously presented) The method of claim 59 further comprising

connecting a central region of said seven-region planar thyristor to a shared row address line.

61. (Previously presented) The method of claim 55 wherein said step of providing doped silicon regions further comprises forming one memory cell.

62. (Currently Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor ~~and to~~ through a write row address line of a memory integrated circuit, said thyristor being adapted to transition from a first one to a second one of said at least two possible current states.

63. (Previously presented) A method of forming a memory integrated circuit comprising:

forming a plurality of thyristor structures over a substrate;

forming a plurality of gates disposed over respective single junctions of said plurality of thyristor structures;

forming a plurality of channels disposed between said thyristor structures, whereby said thyristor structures are disposed in spaced relation to one another; and

mutually coupling at least two gates of said plurality of gates to a write row

address line of said memory integrated circuit.

64. (Previously presented) A method of forming a circuit for storing information as one of at least two possible stable current states as defined in claim 48 wherein said H1 incorporating said multi-region planar thyristor in a memory device comprises coupling said at least one polysilicon gate to a write row address line of said memory device.

65. (Previously presented) A method of forming a device for storing information as one of at least two possible stable current states as defined in claim 55 wherein said incorporating said multi-region planar thyristor in a memory device comprises coupling said at least one polysilicon gate to a write row address line of said memory device.